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Attorney's Docket No. 42P15685
Confirmation No.: 6439

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Scott A. Hareland, et al.

Application No.: 10/607,769

Filed: June 27, 2003

For: Nonplanar Semiconductor Device with
Partially or Fully Wrapped Around Gate
Electrode and Methods of Fabrication

Examiner: Unassigned

Art Unit: 2812

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to MS: Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 29, 2006
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Dianne Neathery
(Typed or printed name of person mailing correspondence)

Dianne Neathery
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Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

- X 37 C.F.R. §1.97(b).
- 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:
- A statement pursuant to 37 C.F.R. §1.97(e) or
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- (1) A statement pursuant to 37 C.F.R. §1.97(e); and
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If there are any additional charges, please charge Deposit Account No.

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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: March 29, 2006


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[illegible]

Examiner Signature		Date Considered	
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Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>			Complete if Known		
			Application Number	10/607,769	
			Filing Date	June 27, 2003	
			First Named Inventor:	Scott A. Hareland, et al.	
			Art Unit	2812	
			Examiner Name	Unassigned	
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FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		Country Code ³	Number ⁴ Kind Code ⁵ (if known)				
		WO	2004/059726 A1	07-15-2004	IBM Corporation		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		International Search Report PCT/US2005/033439, mailed 1/31/2006 (7 pgs.)	
		International Search Report PCT/US2005/035380, mailed 2/13/2006 (14 pgs.)	
		International Search Report PCT/US2005/037169, mailed 2/23/2006 (11 pgs.)	
		SUNG MIN KIM, et al., "A Novel Multi-channel Field Effect Transistr (McFET) on Bulk Si for High Performance Sub-80nm Application, IEDM 04-639, 2004 IEEE, pgs. 27.4.1-27.4.4	
		YANG-KYU CHOI, et al., "A Spacer Patterning Technology for Nanoscale CMOS" IEEE Transactions on Electron Devices, Vol. 49, No. 3, March 2002, pgs. 436-441	
		W. XIONG, et al., "Corner Effect in Multiple-Gate SOI MOSFETs" 2003 IEEE, pgs. 111-113	
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		WEIZE XIONG, et al., "Improvement of FinFET Electrical Characteristics by Hydrogen Annealing" IEEE Electron Device Letters, Vol. 25, No. 8, August 2004, XP-001198998, pgs. 541-543			
		FU-LIANG YANG, et al., "5nm-Gate Nanowire FinFET" 2004 Symposium on VLSI Technology Digest of Technical Papers, 2004 IEEE, pgs. 196-197			
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